said image sensor and said clamp capacitor configured to decrease a difference between impedances of said clamp capacitor in ON and OFF periods.

102. (New) The image system according to claim 78, further comprising a semiconductor substrate including a p^--type impurity base layer and a p^+-type impurity layer formed thereon, and wherein said array of the image sensors is formed in said p^+-type impurity layer.

103. (New) The image system according to claim 78, wherein said sample/hold capacitor and said clamp capacitor are stacked on each other.

104. (New) The image system according to claim 78, wherein said image sensors are two-dimensionally arrayed.

IN THE ABSTRACT

Page 302, paragraph beginning at line 2, please delete in its entirety and insert therefor the following new paragraph:

An image system uses an amplification-type MOS sensor for receiving an optical image through a photoelectric conversion element, converting the image into an electrical signal, and outputting the signal. This system includes an optical system for guiding this optical image to a predetermined position, an image processing means having a sensor for photoelectrically converting the optical image guided to the predetermined position by the optical system into an electrical signal in units of pixels, and a signal process device for processing an output from the image processing means, and outputting the resultant data. The sensor includes a photoelectric conversion element placed at the predetermined position, an output circuit having an amplification MOS transistor connected to the photoelectric conversion element and serving to amplify and output an output from the photoelectric conversion element at a first timing and output noise independent of the output from the